Referring to FIG. 1, a block diagram of a circuit 100 is shown in accordance with a preferred embodiment of the present invention. In one example, the circuit 100 may be implemented as a user programmable wake-up timer. The circuit 100 may implement a programmable wake-up timer that may be used with a processing device, such as a microprocessor or a microcontroller, to control the exiting of a suspend or sleep mode. The circuit 100 may also allow variations in the wake-up time (that may result from processing or operating conditions) to be tuned out. The circuit 100 may allow a user to program a delay value for a wake-up operation. The circuit 100 may have a low-power consumption and may operate in a low-power suspended state without requiring any additional pins or external components.

A1

Please replace the paragraph beginning at page 4, line 7 with the following paragraph:

A2

The circuit 100 may provide a periodic wake-up indication. The circuit 100 may provide the periodic wake-up indication to allow a device (e.g., a computer) to respond to an event (e.g., push of a button or mouse movement). A timing of the wake-up indication may be programmed by a user. The circuit 100 may allow for significant variation and/or adjustment of the wake-up time for different users/applications. The circuit 100 may

provide a reasonable accuracy in sleep time (e.g., efficient use of suspend mode power budget). In the example of a Universal Serial Bus (USB) microcontroller, an average current of less than 500 uA during suspend may be implemented. However, other suspend currents may be implemented accordingly to meet the design criteria of a particular implementation. Additionally, the circuit 100 may be configured to operate between two operating modes. For example, the circuit 100 may operate under any power conditions between a full operation mode and a sleep (or suspend) operation mode (e.g., between (i) a low speed/high speed mode, (ii) a low power/high power mode, etc.). The circuit 100 may eliminate pins previously used for external wake-up components.

Please replace the paragraph beginning at page 6, line 11 with the following paragraph:

In one example, the delay block 102 may be implemented as an analog delay circuit. In another example, the delay circuit 102 may be implemented as a current charging a capacitor, a ring oscillator, and/or a R-C delay time. However, the delay block 102 may be implemented as other types delay devices in order to meet the criteria of a particular implementation. The delay circuit 102 may be implemented as a slow-charging circuit having minimal power consumption. The delay block 102 may be configured to provide a

baseline delay time (e.g., the signal DELAY). The signal DELAY and, therefore, the delay time of the circuit 100 may typically have a wide variation in an integrated circuit application. The variation of the signal DELAY is generally dominated by silicon processing variations in the fabrication of the integrated circuit containing the circuit 100.

Please replace the paragraph beginning at page 12, line 4 with the following paragraph:

The wake-up time of the timer 100 may be tuned (e.g., programmed) by the signal ADJUST[3:1]. Additionally, the wake-up time for a device may be measured during a normal operation (e.g., non-suspended). The measurement of the wake-up time for a particular chip may be accomplished by (i) determining an initial wake-up setting, (ii) starting the wake-up timer 100 (which runs in either awake or suspended modes), (iii) determining a delay time between enabling the wake-up timer 100 and an assertion of the signal OUTPUT and (iv) changing the initial wake-up setting in response to the delay time. The measured wake-up time may indicate a speed of the chip (under the current conditions). The timer 100 may allow a user and/or appropriate firmware to select the best wake-up setting for the particular chip. The wake-up setting may

A4 end

be stored in a register and presented as the signal ADJUST[3:1] during suspend mode (if the circuit is enabled).

Please replace the paragraph beginning at page 14, line 1 with the following paragraph:

A5

The delay circuit 102' may clock the counter 140. The delay counter 102' may clock the counter with the delay clock DELAY. An initial count of the counter 140 may be provided by the signal ADJUST[3:1]. The counter 140 may count UP/DOWN in response to the signal DELAY. The counter 140 may count from the initial value determined from the signal ADJUST[3:1]. The initial value of the signal ADJUST[3:1] may be programmed. Additionally, the initial value may be programmed by a user. When the counter 140 reaches a predetermine value determined by the signal ADJUST[3:1], the counter 140 may assert the signal OUTPUT. For example, the counter 140 may start from an initial value determined by the signal ADJUST[3:1] and count up/down to a target value (e.g., 0 or 7). Additionally, the counter 140 may start from an initial value (e.g., 0 or 8) and count up/down to a target value determined by the signal ADJUST[3:1].